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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/701,321	11/04/2003	Joung-Yeal Kim	5649-1169	5300
20792	7590	08/18/2005	EXAMINER	
MYERS BIGEL SIBLEY & SAJOVEC			TRAN, ANH Q	
PO BOX 37428			ART UNIT	
RALEIGH, NC 27627			PAPER NUMBER	

2819

DATE MAILED: 08/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/701,321

Applicant(s)

KIM, JOUNG-YEAL

Examiner

Anh Q. Tran

Art Unit

2819

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 June 2005.
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,3-13,15-24 and 41-49 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☒ Claim(s) 1,3-13 and 15-24 is/are allowed.
6) ☒ Claim(s) 41 is/are rejected.
7) ☒ Claim(s) 42-49 is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. Claim 41 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moyal (6,329,840) in view of Rhyne (Fundamentals of Digital Systems Design, N.J., 1973, pp. 70-71).

Moyal discloses a pull-up transistor (M17) which pulls up an output terminal (124);

A pull-down transistor (M18) which pulls down the output terminal;

wherein a number of PMOS transistors (M9-M10) present along a path of a first supply voltage to an output terminal of the NAND gate is equivalent to a number of PMOS transistors (M1-M2) present along a path of the first supply voltage to an output terminal of the NOR gate, and a number of NMOS transistors (M11-M12) present along a path of a second supply voltage to an output terminal of the NAND gate is equivalent to a number of NMOS transistors (M3-M4) present along a path of the second supply voltage to an output terminal of the NOR gate. Moyal discloses the claimed invention except for the NAND gate connected to the pull-up transistor and the NOR gate connected to the pull-down transistor instead of the NOR gate connected to the pull-up transistor and the NAND gate connected to the pull-down transistor .

Rhyne teaches a function of any one of the four logical functions, AND, OR, NAND, or NOR, can be redefined so as to perform the other three (Fig. 3-10), these function is equivalent structure known in the art

Therefore, because these two gate function as NOR gate or NAND gate were art-recognized equivalents at the time the invention was made, one of ordinary skill in the art would have found it obvious to substitute the NAND gate connected to the pull-up transistor and the NOR gate connected to the pull-down transistor for the NOR gate connected to the pull-up transistor and the NAND gate connected to the pull-down transistor.

Allowable Subject Matter

2. Claims 42-49 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

3. Claims 1, 3-13, 15-24 are allowed.

4. The following is an examiner's statement of reasons for allowance: with respect to the claims the prior fails to teach or disclose the applicant's invention as claimed, particularly the feature describing

- wherein the plurality of serially connected transistors in the electrical path between the supply voltage and the first output node comprises a first transistor having a first control electrode connected to the data signal and a second transistor coupled in series between the supply voltage and the first transistors the first logic gate further comprising a third transistor connected in parallel with the first transistor between the second transistor and the first output node,

wherein the third transistor has a third control electrode connected to the control signal.

- wherein the plurality of serially connected transistors in the electrical path between the second output node and the reference voltage comprises a first transistor having a first control electrode connected to the data signal and a second transistor connected in series between the first transistor and the reference voltage, the second logic gate further comprising a third transistor connected in parallel with the first transistor between the second transistor and the second output nodes wherein the third transistor has a control electrode connected to the inverse of the control signal.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh Q. Tran whose telephone number is 571-272-1813. The examiner can normally be reached on M-TH (7:00-5:30) Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on 571-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANH Q. TRAN
PRIMARY EXAMINER



Handwritten signature of Anh Q. Tran, dated 8/16/05.

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